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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/754,926	01/12/2004	Yukihiro Noguchi	65933-065	8354

7590 09/20/2005

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EXAMINER	
TRAN, ANH Q	

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 09/20/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/754,926	NOGUCHI ET AL.	
	Examiner	Art Unit	
	Anh Q. Tran	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 September 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-36* is/are pending in the application.

4a) Of the above claim(s) *5,7-31,35 and 36* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6 and 32-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4/26/04, 7/8/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This application contains claims 5, 7, 18 and 19 drawn to an invention nonelected. Claims 5, 7, 18 and 19 are withdrawn from further consideration pursuant to 37 CFR 1.142(b), as being drawn to a nonelected figures. Applicants elected to prosecute Species I, directed to the Fig. 5 embodiment but claims 5, 7, 18 and 19 includes elements of nonelected figures that are not shown in figure 5.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-4, 6, 32 are rejected under 35 U.S.C. 102(b) as being anticipated by Koyada Hiroshi (JP-06-037624).

Hiroshi shows:

1. A level conversion circuit (Fig. 1), comprising:

a first transistor of a first conductive type (M12) which is connected between a supply node (VDD) to which supply voltage is impressed and an output node (A); and a second transistor (M22) of a second conductive type which is connected between an input node (IN) to which an input signal is inputted and the output node, wherein a control electrode (gate of M22 is connected to VDD) of the second transistor is connected to the supply node and a control electrode of the first transistor is connected to an output (OUT) of a prescribed circuit (M13 and M23) and to which the input signal

is inputted (inputted through gate M23), wherein an output signal is obtained from the output node.

2-4. A level conversion circuit according to Claim 1, wherein the single supply voltage (VDD) is set for the first and second transistors or the different supply voltages are and second transistors, separately set for the first wherein the supply voltage which corresponds to the first transistor is set to a value higher than high level (VDD is higher voltage than VCC which correspond to input signal) of the input signal and the supply voltage which corresponds to the second transistor is set to a higher value than high level (VDD is higher voltage than VCC which correspond to input signal) of the input signal, wherein degree of ON status of the first and second transistors is controlled according to difference between the supply voltages and voltage of the input signal, and wherein the input signal is converted to the output signal corresponding to the supply voltage (VDD).

6. A level conversion circuit according to Claim 1, wherein the prescribed circuit is an inverter circuit (M13 and M23 is an inverter).

32. A level conversion circuit according to Claim 1, wherein the output signal is adjusted to have target voltage Vm = (VG + VDD) / 2 as center of amplitude thereof when the ground voltage and the supply voltage are respectively described as VG and VDD (inherent limitation of target volt between supply voltage and ground).

3. Claims 1-4, 6, 32-33 are rejected under 35 U.S.C. 102(b) as being anticipated by Nakano (5,387,828).

Nakano shows:

1. A level conversion circuit (Fig. 3), comprising:

a first transistor of a first conductive type (QP11) which is connected between a supply node (VDD) to which supply voltage is impressed and an output node (D11); and a second transistor (Qn12) of a second conductive type which is connected between an input node (14a) to which an input signal is inputted and the output node, wherein a control electrode of the second transistor is connected to the supply node and a control electrode of the first transistor is connected to an output (14b) of a prescribed circuit (inverter circuit is prescribed circuit which is inherent element that provide complementary to 14b, col. 4, lines 16-18) and to which the input signal is inputted, wherein an output signal is obtained from the output node.

2-4. A level conversion circuit according to Claim 1, wherein the single supply voltage (VDD) is set for the first and second transistors or the different supply voltages are and second transistors, separately set for the first wherein the supply voltage which corresponds to the first transistor is set to a value higher than high level (VDD is higher voltage than input signal voltage, see Fig. 4A) of the input signal and the supply voltage which corresponds to the second transistor is set to a higher value than high level (VDD is higher voltage than input signal voltage, see Fig. 4A) of the input signal, wherein degree of ON status of the first and second transistors is controlled according to difference between the supply voltages and voltage of the input signal, and wherein the input signal is converted to the output signal corresponding to the supply voltage (VDD).

6. A level conversion circuit according to Claim 1, wherein the prescribed circuit is an inverter circuit (inherent element of complementary input node).

32. A level conversion circuit according to Claim 1, wherein the output signal is adjusted to have target voltage Vm = (VG + VDD) / 2 as center of amplitude thereof when the ground voltage and the supply voltage are respectively described as VG and VDD (inherent limitation of target volt between supply voltage and ground).

33. A level conversion circuit according to Claim 32 characterized in that further comprises a buffer circuit (12) which has the target voltage Vm as a central point of operation, and amplitude of output of which covers from voltage close to the ground voltage to voltage close to the supply voltage, wherein a modified output signal (15a) is obtained by passing the output signal through the buffer circuit.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claim 34 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nakano (5,387,828).

Nakano discloses the claimed invention except for the transistors are made of polycrystalline silicon. It would have been obvious to one having ordinary skill in the art at the time the invention was made to have the transistors made of polycrystalline silicon, since it has been held to be within the general skill of a worker in the art to select

a known material on the basis of its suitability for the intended use as a matter of obvious design choice.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

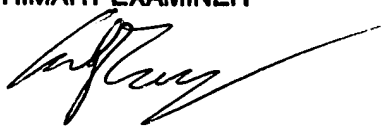
Tanzawa (6,344,764) discloses a level shifting circuit with input node is inputting at the source terminal of a transistor.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anh Q. Tran whose telephone number is 571-272-1813. The examiner can normally be reached on M-TH (7:00-5:30) Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Pascal can be reached on 571-272-1769. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ANH Q. TRAN
PRIMARY EXAMINER



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